# 10 µA, Rail-to-Rail I/O, Zero Input Crossover Distortion Amplifiers

# ADA4505-1/ADA4505-2/ADA4505-4

## FEATURES

**PSRR: 100 dB minimum**
**CMRR: 105 dB typical**
**Very low supply current: 10 µA per amplifier maximum**
**1.8 V to 5 V single-supply or ±0.9 V to ±2.5 V dual-supply operation**
**Rail-to-rail input and output**
**3 mV offset voltage maximum**
**Very low input bias current: 0.5 pA typical**

## APPLICATIONS

**Pressure and position sensors**
**Remote security**
**Medical monitors**
**Battery-powered consumer equipment**
**Hazard detectors**

## GENERAL DESCRIPTION

The ADA4505-1/ADA4505-2/ADA4505-4 are single, dual, and quad micropower amplifiers featuring rail-to-rail input and output swings while operating from a single 1.8 V to 5 V power supply or from dual ±0.9 V to ±2.5 V power supplies.

Employing a new circuit technology, these low cost amplifiers offer zero input crossover distortion (excellent PSRR and CMRR performance) and very low bias current, while operating with a supply current of less than 10 µA per amplifier.

This combination of features makes the ADA4505-x amplifiers ideal choices for battery-powered applications because they minimize errors due to power supply voltage variations over the lifetime of the battery and maintain high CMRR even for a rail-to-rail op amp.

Remote battery-powered sensors, handheld instrumentation and consumer equipment, hazard detectors (for example, smoke, fire, and gas), and patient monitors can benefit from the features of the ADA4505-x amplifiers.

The ADA4505-x family is specified for both the industrial temperature range (−40°C to +85°C) and the extended industrial temperature range (−40°C to +125°C). The ADA4505-1 single amplifier is available in a tiny 5-lead SOT-23. The ADA4505-2 dual amplifier is available in a standard 8-lead MSOP and a 8-ball WLCSP. The ADA4505-4 quad amplifier is available in a 14-lead TSSOP and a 14-ball WLCSP.

The ADA4505-x family is a member of a growing series of zero crossover op amps offered by Analog Devices, Inc., including the AD8506/AD8508, which also operate from a single 1.8 V to 5 V power supply or from dual ±0.9 V to ±2.5 V power supplies.

## PIN CONFIGURATIONS

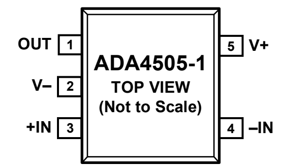

*Figure 1. 5-Lead SOT-23 (RJ-5)*

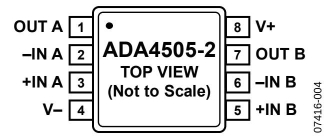

*Figure 2. 8-Lead MSOP (RM-8)*

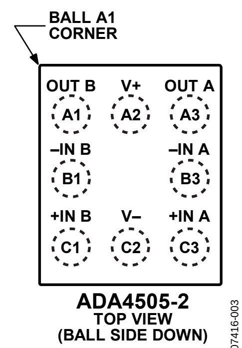

*Figure 3. 8-Ball WLCSP (CB-8-2)*

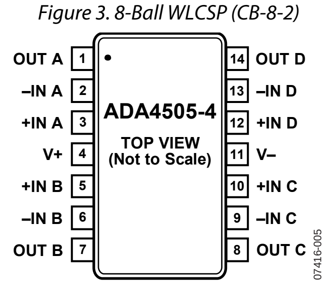

*Figure 4. 14-Lead TSSOP (RU-14)*

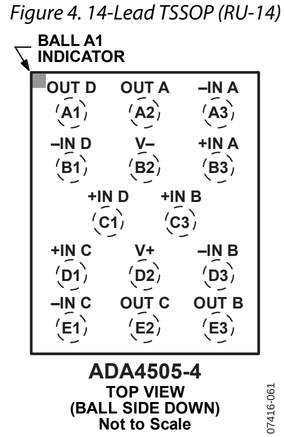

*Figure 5. 14-Ball WLCSP (CB-14-1)*




**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700 www.analog.com**
**Fax: 781.461.3113**

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## REVISION HISTORY

**7/09—Rev. B to Rev. C**

Added 5-Lead SOT-23 (ADA4505-1) ... Throughout
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Changes to Figure 26 and Figure 29 ... 9
Changes to Figure 31 and Figure 34 ... 10
Changes to Figure 42 and Figure 45 ... 12
Added Figure 49 and Figure 51; Renumbered Sequentially ... 13
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 20

**2/09—Rev. A to Rev. B**

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Updated Outline Dimensions ... 18
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**10/08—Rev. 0 to Rev. A**

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**7/08—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—5 V OPERATION

$V_{SY}$ = 5 V, $V_{CM}$ = $V_{SY}$/2, $T_A$ = 25°C, $R_L$ = 100 kΩ to GND, unless otherwise specified.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | 0 V ≤ $V_{CM}$ ≤ 5 V | | 0.5 | 3 | mV |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 4 | mV |
| Input Bias Current | $I_B$ | | | 0.5 | 2 | pA |
| | | −40°C ≤ $T_A$ ≤ +85°C | | | 50 | pA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 375 | pA |
| Input Offset Current | $I_{OS}$ | | | 0.05 | 1 | pA |
| | | −40°C ≤ $T_A$ ≤ +85°C | | | 25 | pA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 130 | pA |
| Input Voltage Range | | −40°C ≤ $T_A$ ≤ +125°C | 0 | | 5 | V |
| Common-Mode Rejection Ratio | CMRR | 0 V ≤ $V_{CM}$ ≤ 5 V | 90 | 105 | | dB |
| | | −40°C ≤ $T_A$ ≤ +85°C | 90 | | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 85 | | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | 0.05 V ≤ $V_{OUT}$ ≤ 4.95 V | 105 | 120 | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 100 | | | dB |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | −40°C ≤ $T_A$ ≤ +125°C | | 2 | | μV/°C |
| Input Resistance | $R_{IN}$ | | | 220 | | GΩ |
| Input Capacitance Differential Mode | $C_{INDM}$ | | | 2.5 | | pF |
| Input Capacitance Common Mode | $C_{INCM}$ | | | 4.7 | | pF |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | $R_L$ = 100 kΩ to GND | 4.98 | 4.99 | | V |
| | | −40°C ≤ $T_A$ ≤ +125°C | 4.98 | | | V |
| | | $R_L$ = 10 kΩ to GND | 4.9 | 4.95 | | V |
| | | −40°C ≤ $T_A$ ≤ +125°C | 4.9 | | | V |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 100 kΩ to $V_{SY}$ | | 2 | 5 | mV |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 5 | mV |
| | | $R_L$ = 10 kΩ to $V_{SY}$ | | 10 | 25 | mV |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 25 | mV |
| Short-Circuit Limit | $I_{SC}$ | $V_{OUT}$ = $V_{SY}$ or GND | | ±40 | | mA |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY}$ = 1.8 V to 5 V | 100 | 110 | | dB |
| | | −40°C ≤ $T_A$ ≤ +85°C | 100 | | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 95 | | | dB |
| Supply Current per Amplifier | $I_{SY}$ | $V_{OUT}$ = $V_{SY}$/2 | | | | |
| ADA4505-1 | | | | 9 | 10.5 | μA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 15 | μA |
| ADA4505-2/ADA4505-4 | | | | 7 | 10 | μA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 15 | μA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 100 kΩ, $C_L$ = 20 pF, G = 1 | | 6 | | mV/μs |
| Gain Bandwidth Product | GBP | $R_L$ = 1 MΩ, $C_L$ = 20 pF, G = 1 | | 50 | | kHz |
| Phase Margin | $\Phi_M$ | $R_L$ = 1 MΩ, $C_L$ = 20 pF, G = 1 | | 52 | | Degrees |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | $e_n$ p-p | f = 0.1 Hz to 10 Hz | | 2.95 | | μV p-p |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 65 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 1 kHz | | 20 | | fA/√Hz |

## ELECTRICAL CHARACTERISTICS—1.8 V OPERATION

$V_{SY}$ = 1.8 V, $V_{CM}$ = $V_{SY}/2$, $T_A$ = 25°C, $R_L$ = 100 kΩ to GND, unless otherwise specified.

**Table 2.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | 0 V ≤ $V_{CM}$ ≤ 1.8 V | | 0.5 | 3 | mV |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 4 | mV |
| Input Bias Current | $I_B$ | | | 0.5 | 2 | pA |
| | | −40°C ≤ $T_A$ ≤ +85°C | | | 50 | pA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 375 | pA |
| Input Offset Current | $I_{OS}$ | | | 0.05 | 1 | pA |
| | | −40°C ≤ $T_A$ ≤ +85°C | | | 25 | pA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 130 | pA |
| Input Voltage Range | | −40°C ≤ $T_A$ ≤ +125°C | 0 | | 1.8 | V |
| Common-Mode Rejection Ratio | CMRR | 0 V ≤ $V_{CM}$ ≤ 1.8 V | 85 | 100 | | dB |
| | | −40°C ≤ $T_A$ ≤ +85°C | 85 | | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 80 | | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | 0.05 V ≤ $V_{OUT}$ ≤ 1.75 V | 95 | 115 | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 95 | | | dB |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | −40°C ≤ $T_A$ ≤ +125°C | | 2.5 | | μV/°C |
| Input Resistance | $R_{IN}$ | | | 220 | | GΩ |
| Input Capacitance Differential Mode | $C_{INDM}$ | | | 2.5 | | pF |
| Input Capacitance Common Mode | $C_{INCM}$ | | | 4.7 | | pF |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | $R_L$ = 100 kΩ to GND | 1.78 | 1.79 | | V |
| | | −40°C ≤ $T_A$ ≤ +125°C | 1.78 | | | V |
| | | $R_L$ = 10 kΩ to GND | 1.65 | 1.75 | | V |
| | | −40°C ≤ $T_A$ ≤ +125°C | 1.65 | | | V |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 100 kΩ to $V_{SY}$ | | 2 | 5 | mV |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 5 | mV |
| | | $R_L$ = 10 kΩ to $V_{SY}$ | | 12 | 25 | mV |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 25 | mV |
| Short-Circuit Limit | $I_{SC}$ | $V_{OUT}$ = $V_{SY}$ or GND | | ±3.8 | | mA |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY}$ = 1.8 V to 5 V | 100 | 110 | | dB |
| | | −40°C ≤ $T_A$ ≤ +85°C | 100 | | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 95 | | | dB |
| Supply Current per Amplifier | $I_{SY}$ | $V_{OUT}$ = $V_{SY}/2$ | | | | |
| ADA4505-1 | | | | 10 | 11.5 | μA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 15 | μA |
| ADA4505-2/ADA4505-4 | | | | 7 | 10 | μA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 15 | μA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 100 kΩ, $C_L$ = 20 pF, G = 1 | | 6.5 | | mV/μs |
| Gain Bandwidth Product | GBP | $R_L$ = 1 MΩ, $C_L$ = 20 pF, G = 1 | | 50 | | kHz |
| Phase Margin | $\Phi_M$ | $R_L$ = 1 MΩ, $C_L$ = 20 pF, G = 1 | | 52 | | Degrees |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | $e_n$ p-p | f = 0.1 Hz to 10 Hz | | 2.95 | | μV p-p |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 65 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 1 kHz | | 20 | | fA/√Hz |

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 5.5 V |
| Input Voltage | $\pm V_{SY} \pm 0.1$ V |
| Input Current[1] | ±10 mA |
| Differential Input Voltage[2] | $\pm V_{SY}$ |
| Output Short-Circuit Duration to GND | Indefinite |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +125°C |
| Junction Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 60 sec) | 300°C |

[1] Input pins have clamp diodes to the supply pins. Limit input current to 10 mA or less whenever the input signal exceeds the power supply rail by 0.1 V.
[2] Differential input voltage is limited to 5 V or the supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a standard 4-layer board, unless otherwise specified.

**Table 4.**

| Package Type | $\theta_{JA}$ | $\theta_{JB}$[1] | $\theta_{JC}$ | Unit |
|---|---|---|---|---|
| 5-Lead SOT-23 (RJ-5) | 190 | N/A | 92 | °C/W |
| 8-Lead MSOP (RM-8) | 206 | N/A | 44 | °C/W |
| 8-Ball WLCSP (CB-8-2) | | | | |
| 2-Layer PCB (1SOP)[2] | 178 | 42 | N/A | °C/W |
| 4-Layer PCB (2S2P)[2] | 82 | 23 | N/A | °C/W |
| 14-Lead TSSOP (RU-14) | 112 | N/A | 35 | °C/W |
| 14-Ball WLCSP (CB-14-1) | | | | |
| 2-Layer PCB (1SOP)[2] | 130 | 23 | N/A | °C/W |
| 4-Layer PCB (2S2P)[2] | 64 | 15 | N/A | °C/W |

[1] Junction-to-board thermal resistance.
[2] Simulated thermal numbers per JESD51-9 follow:
2-layer PCB (1SOP); low effective thermal conductivity test board
4-layer PCB (2S2P); high effective thermal conductivity test board

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

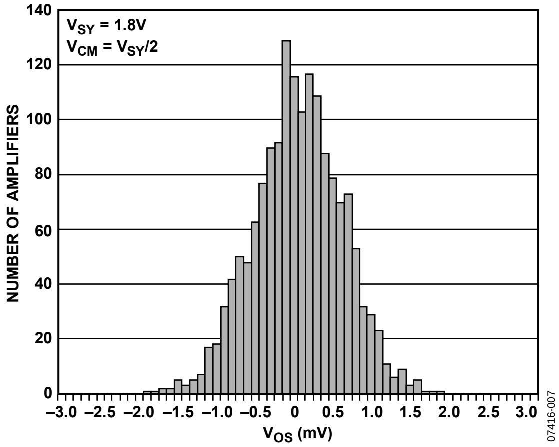



Figure 6. Input Offset Voltage Distribution

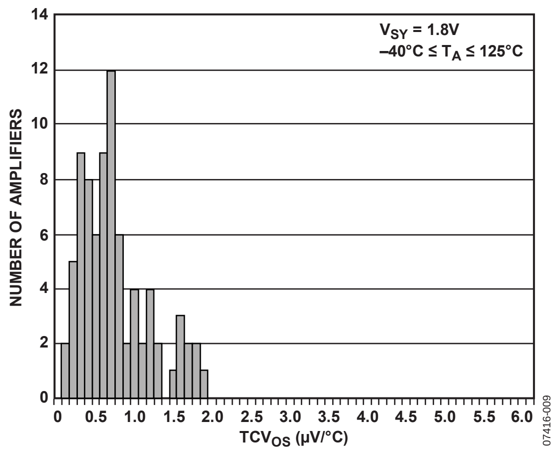



Figure 7. Input Offset Voltage Drift Distribution

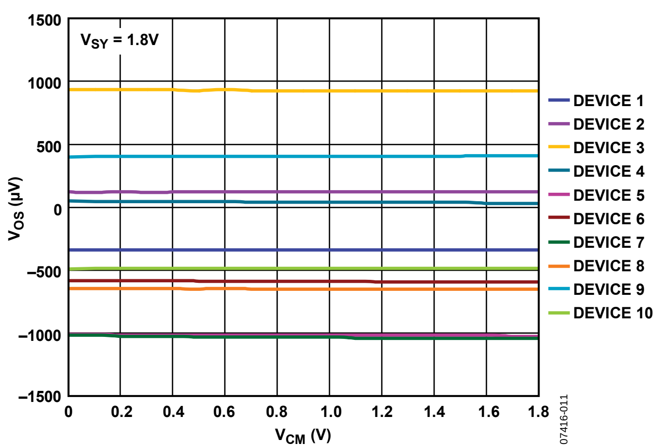



Figure 8. Input Offset Voltage vs. Common-Mode Voltage

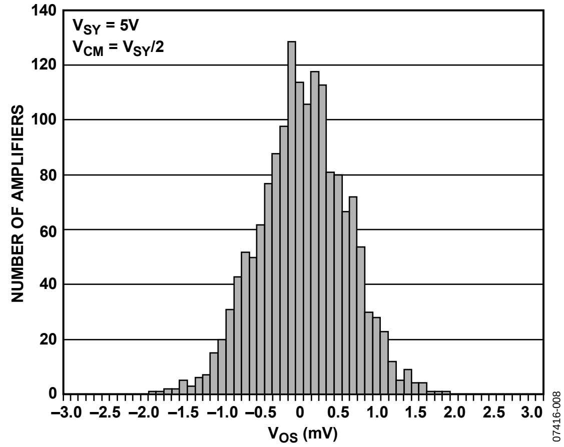



Figure 9. Input Offset Voltage Distribution

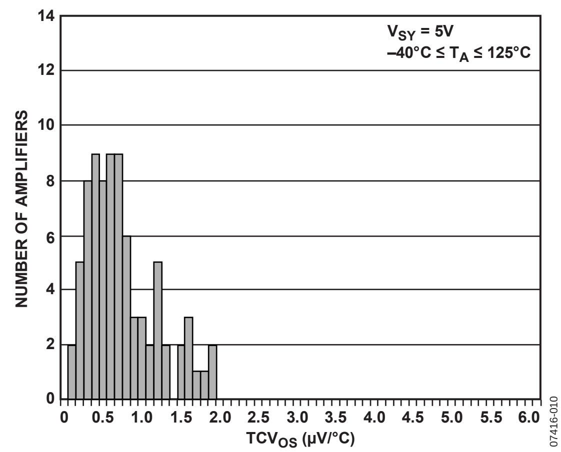



Figure 10. Input Offset Voltage Drift Distribution

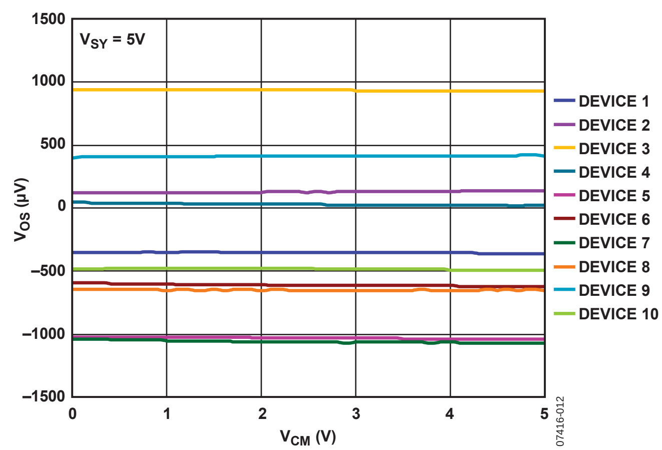



Figure 11. Input Offset Voltage vs. Common-Mode Voltage

$T_A$ = 25°C, unless otherwise noted.

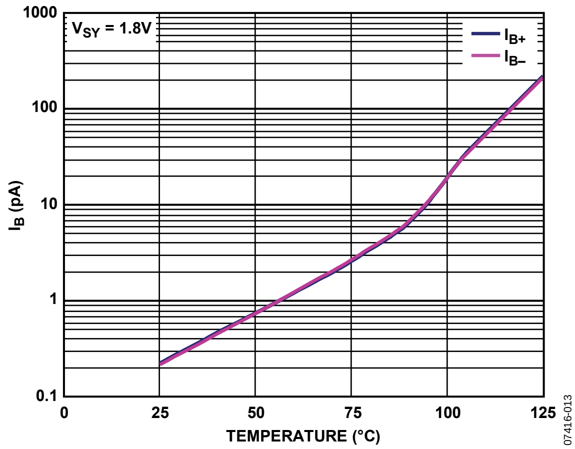



*Figure 12. Input Bias Current vs. Temperature*

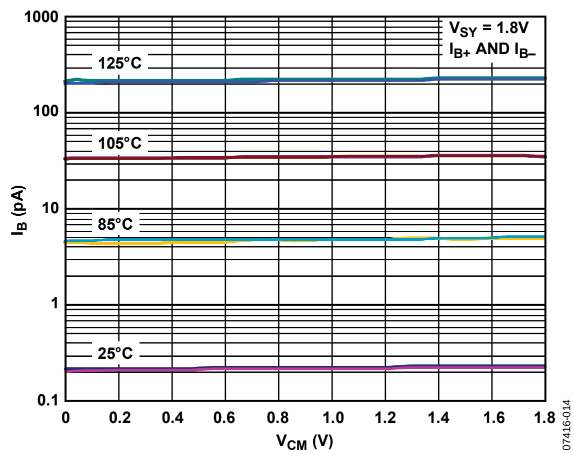



*Figure 13. Input Bias Current vs. Common-Mode Voltage and Temperature*

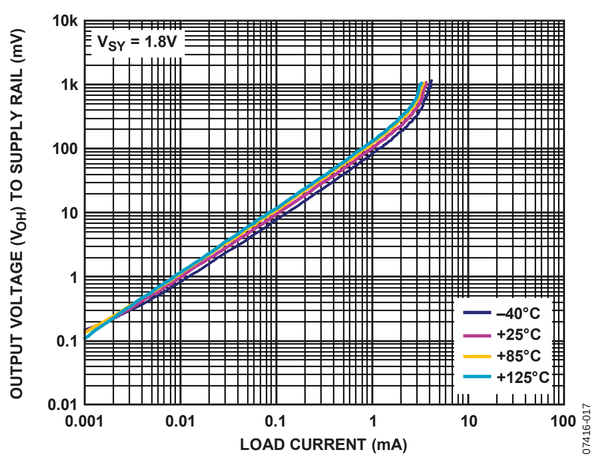



*Figure 14. Output Voltage ($V_{OH}$) to Supply Rail vs. Load Current and Temperature*

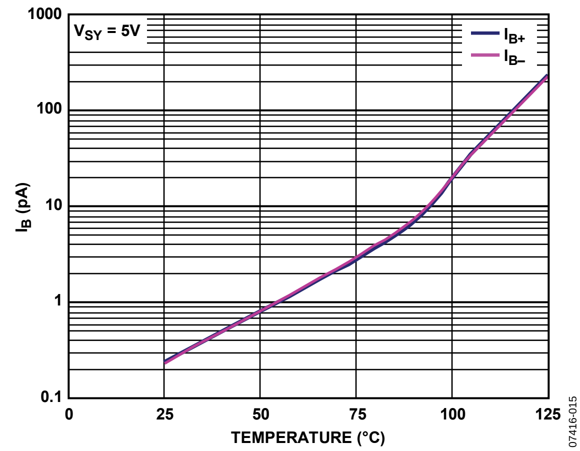



*Figure 15. Input Bias Current vs. Temperature*

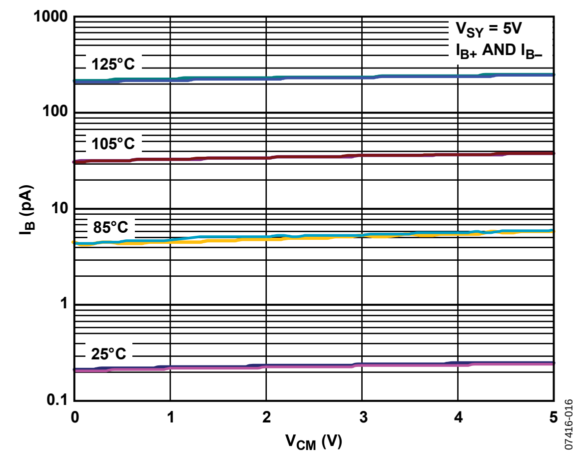



*Figure 16. Input Bias Current vs. Common-Mode Voltage and Temperature*

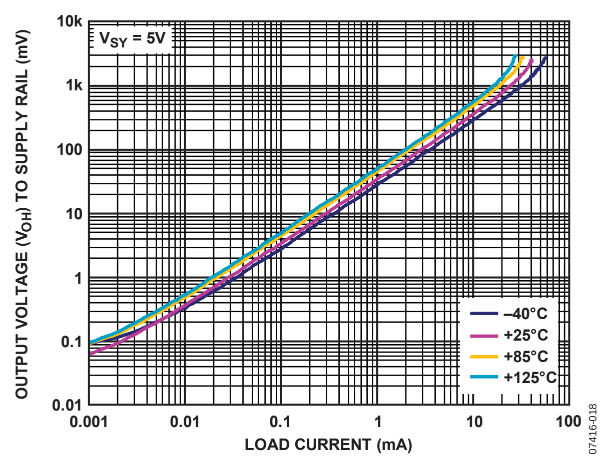



*Figure 17. Output Voltage ($V_{OH}$) to Supply Rail vs. Load Current and Temperature*

$T_A$ = 25°C, unless otherwise noted.

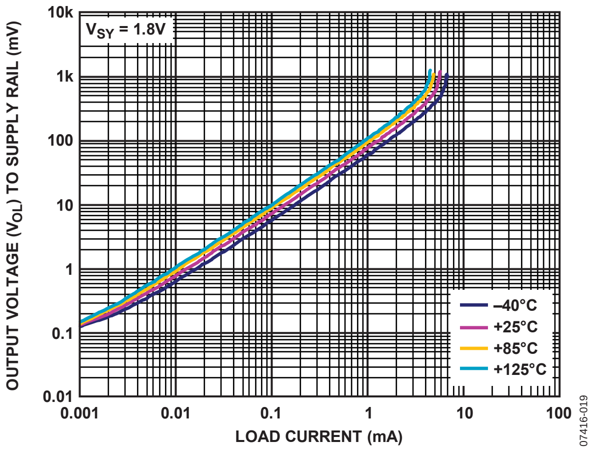



Figure 18. Output Voltage ($V_{OL}$) to Supply Rail vs. Load Current and Temperature

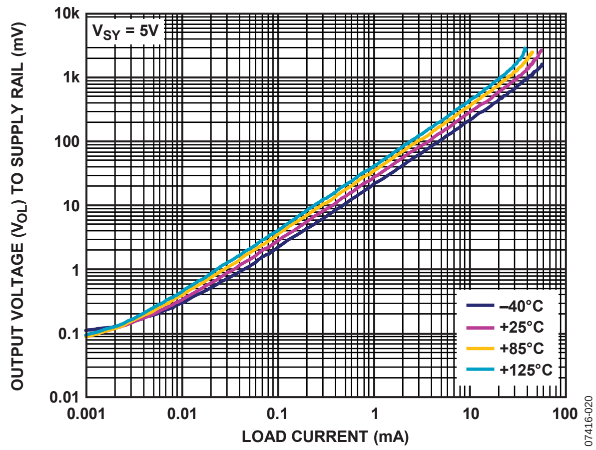



Figure 21. Output Voltage ($V_{OL}$) to Supply Rail vs. Load Current and Temperature

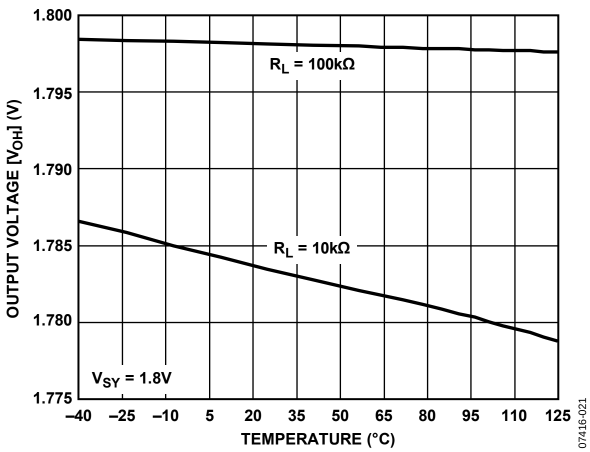



Figure 19. Output Voltage ($V_{OH}$) vs. Temperature

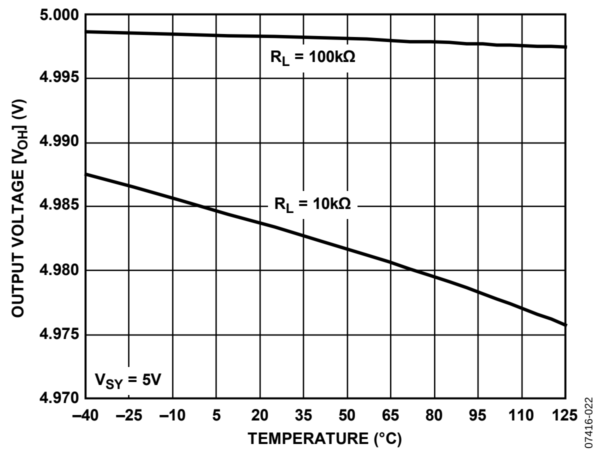



Figure 22. Output Voltage ($V_{OH}$) vs. Temperature

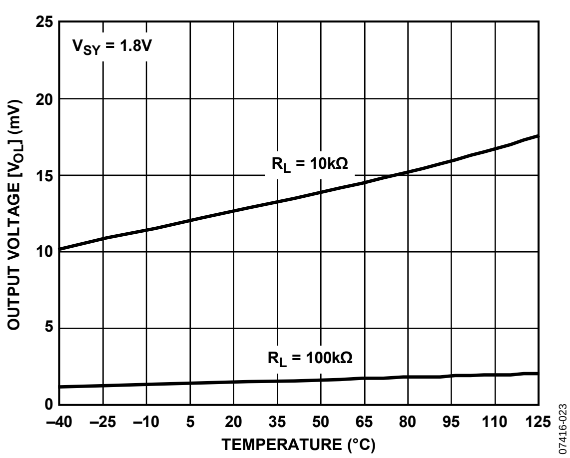



Figure 20. Output Voltage ($V_{OL}$) vs. Temperature

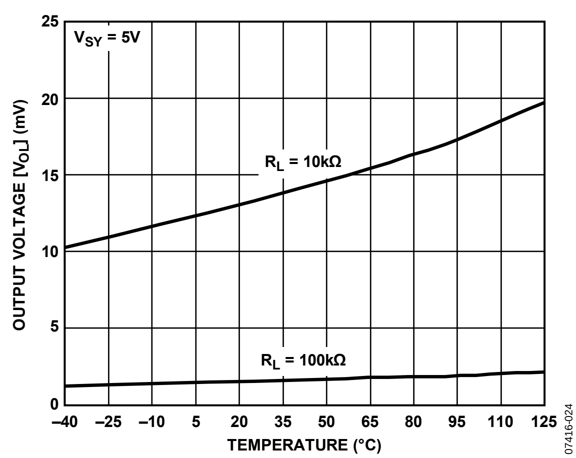



Figure 23. Output Voltage ($V_{OL}$) vs. Temperature

$T_A$ = 25°C, unless otherwise noted.

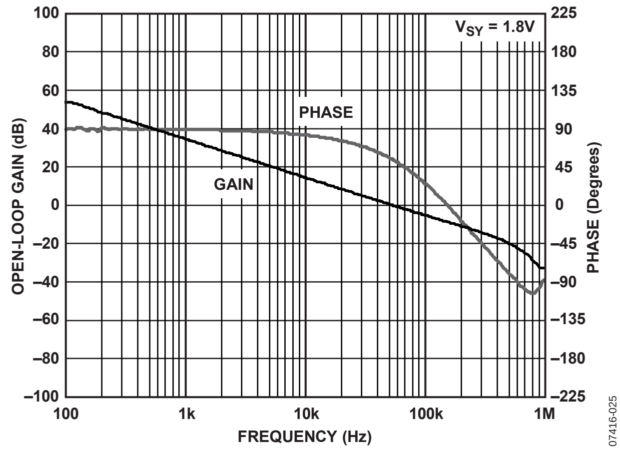



Figure 24. Open-Loop Gain and Phase vs. Frequency

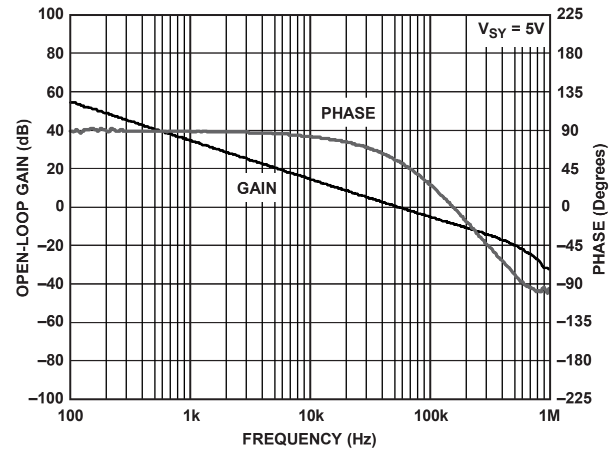



Figure 27. Open-Loop Gain and Phase vs. Frequency

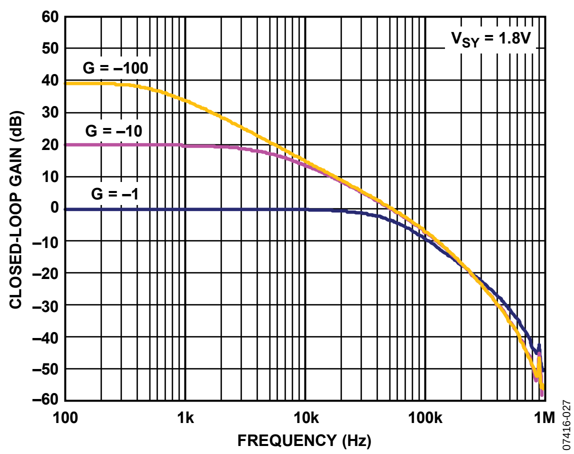



Figure 25. Closed-Loop Gain vs. Frequency

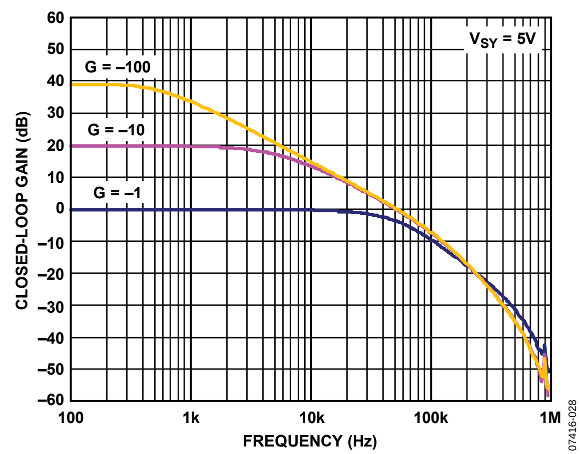



Figure 28. Closed-Loop Gain vs. Frequency

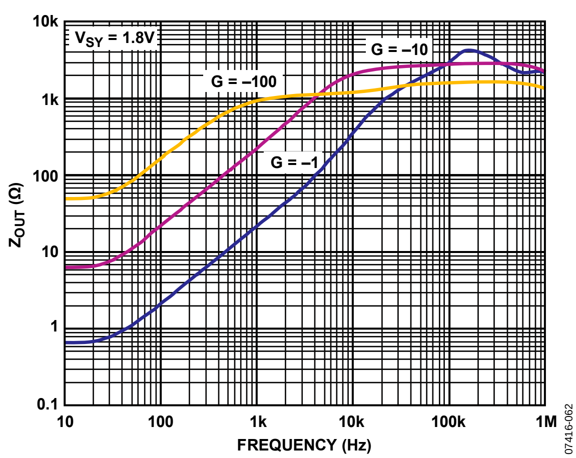



Figure 26. Output Impedance vs. Frequency

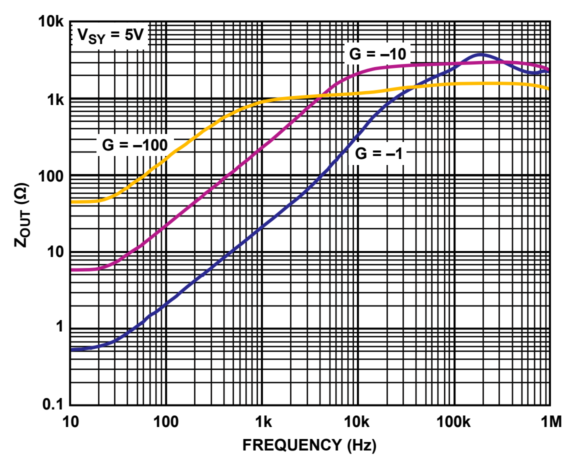



Figure 29. Output Impedance vs. Frequency

$T_A$ = 25°C, unless otherwise noted.

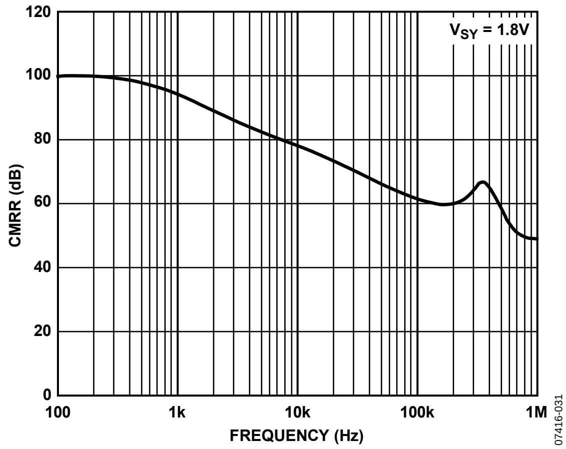



Figure 30. CMRR vs. Frequency

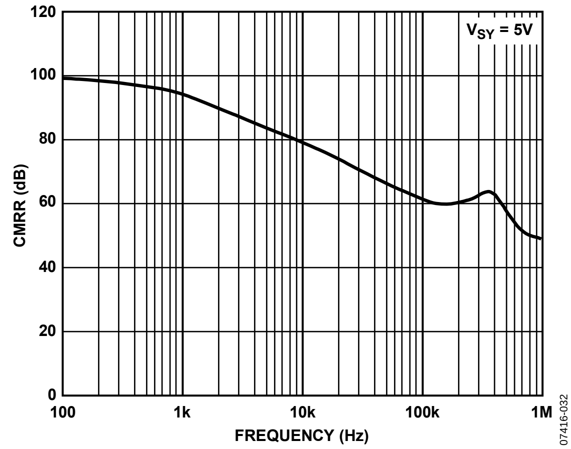



Figure 33. CMRR vs. Frequency

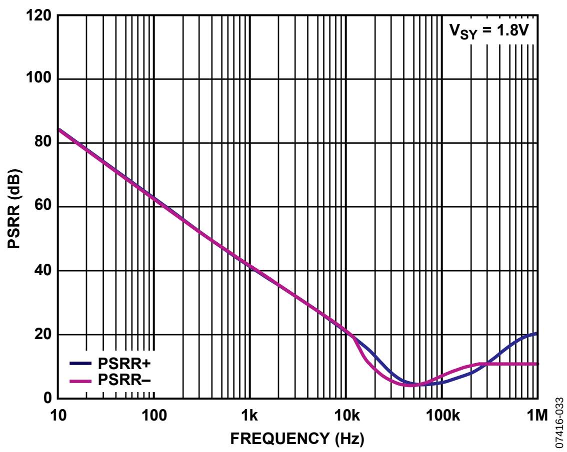



Figure 31. PSRR vs. Frequency

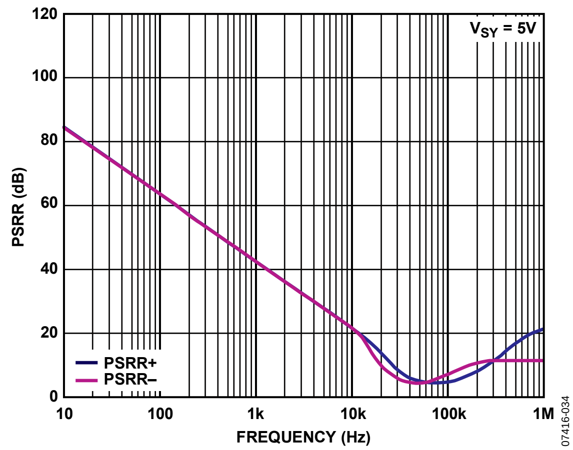



Figure 34. PSRR vs. Frequency

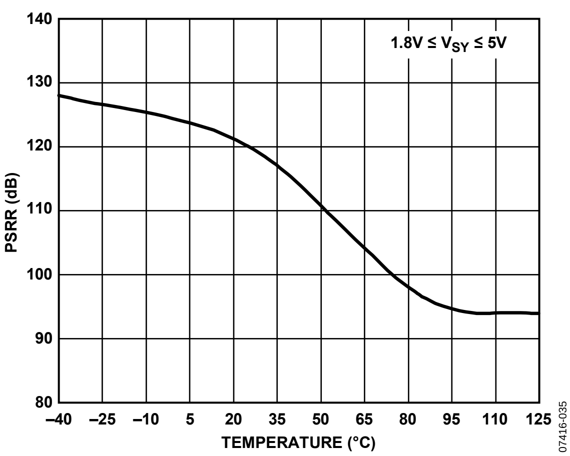



Figure 32. PSRR vs. Temperature

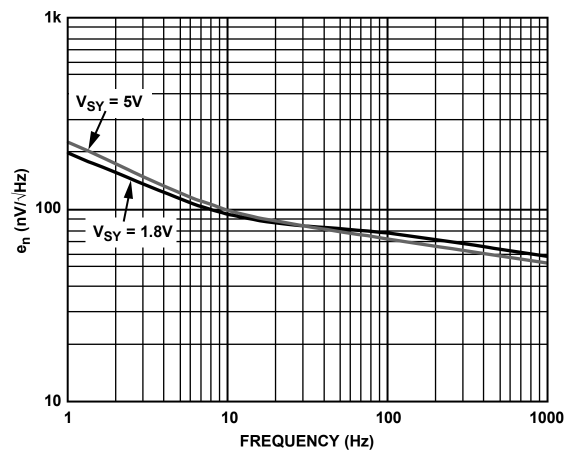



Figure 35. Voltage Noise Density vs. Frequency

$T_A$ = 25°C, unless otherwise noted.

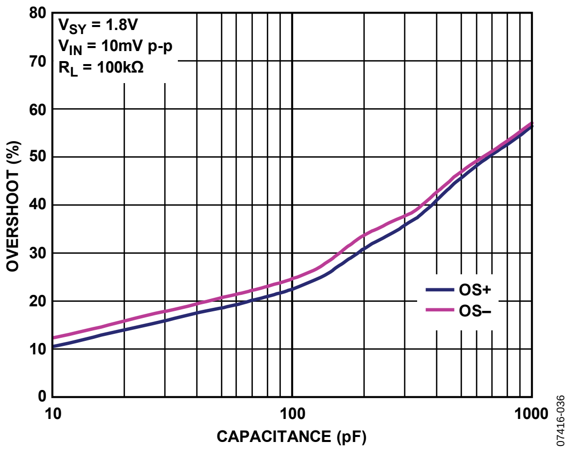



*Figure 36. Small Signal Overshoot vs. Load Capacitance*

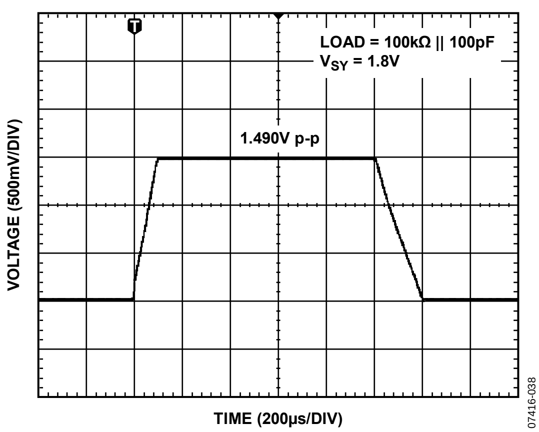



*Figure 37. Large Signal Transient Response*

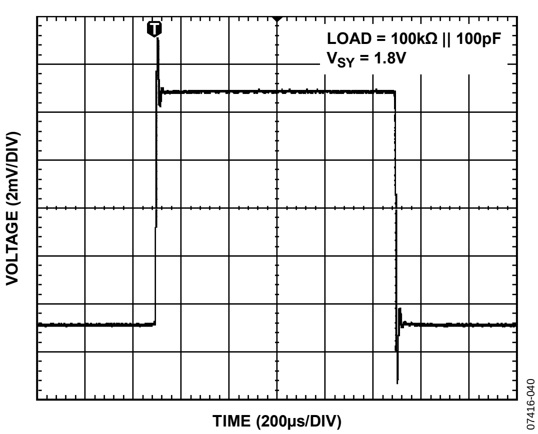



*Figure 38. Small Signal Transient Response*

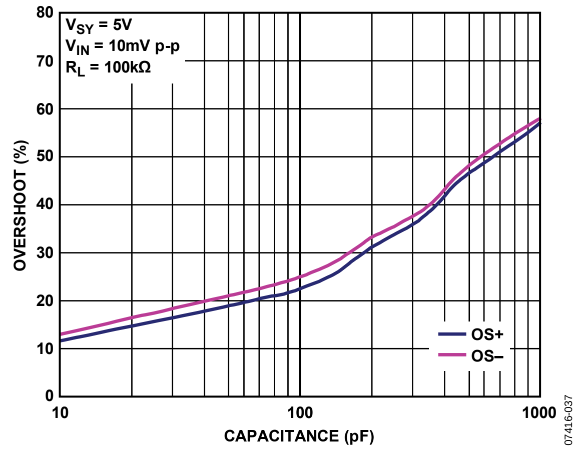



*Figure 39. Small Signal Overshoot vs. Load Capacitance*

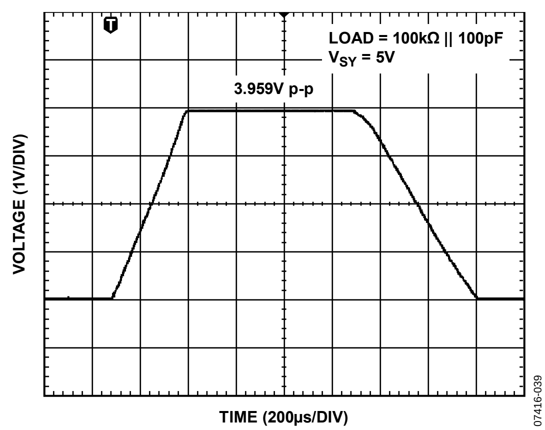



*Figure 40. Large Signal Transient Response*

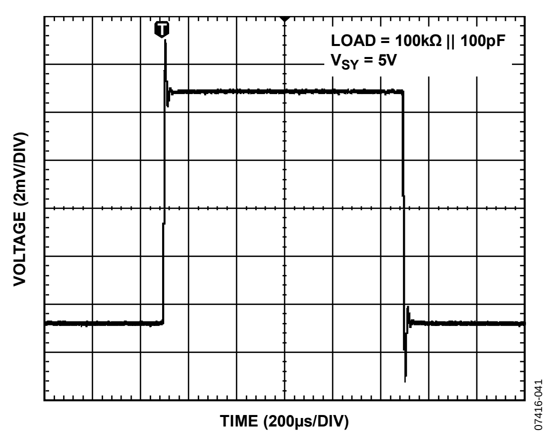



*Figure 41. Small Signal Transient Response*

$T_A$ = 25°C, unless otherwise noted.

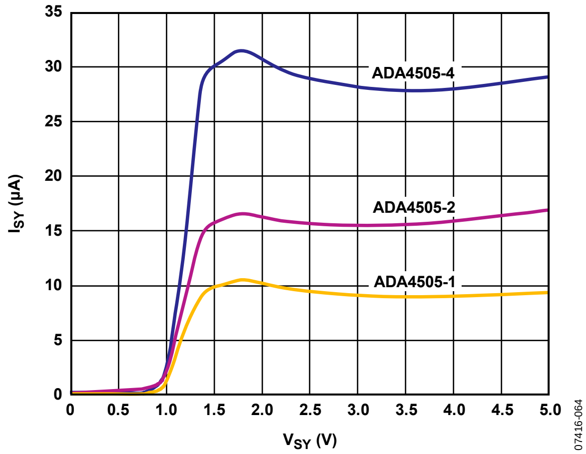



Figure 42. Supply Current vs. Supply Voltage

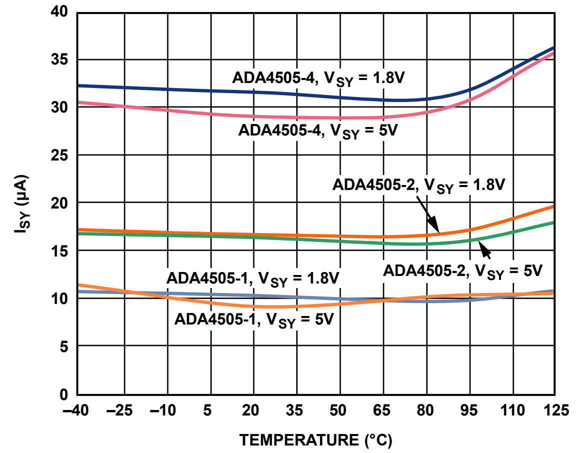



Figure 45. Total Supply Current vs. Temperature

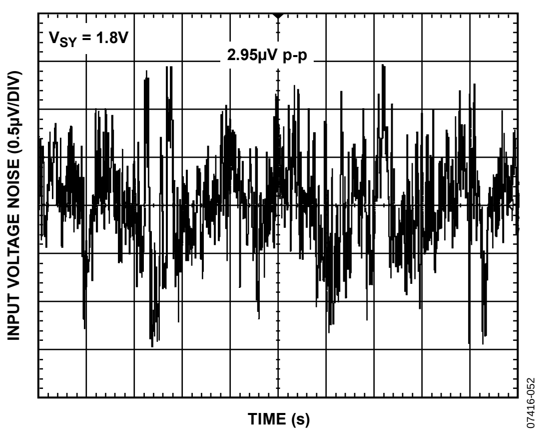



Figure 43. Input Voltage Noise, 0.1 Hz to 10 Hz Noise

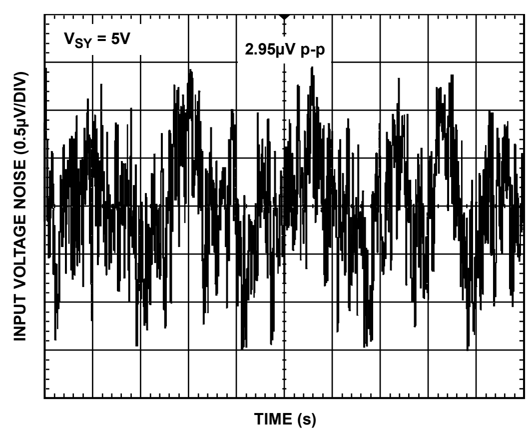



Figure 46. Input Voltage Noise, 0.1 Hz to 10 Hz Noise

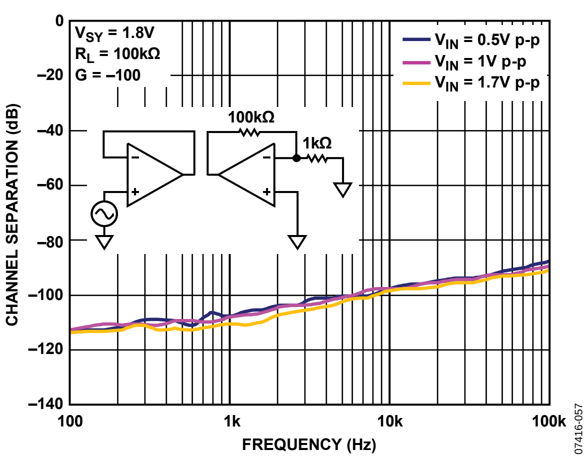



Figure 44. Channel Separation vs. Frequency

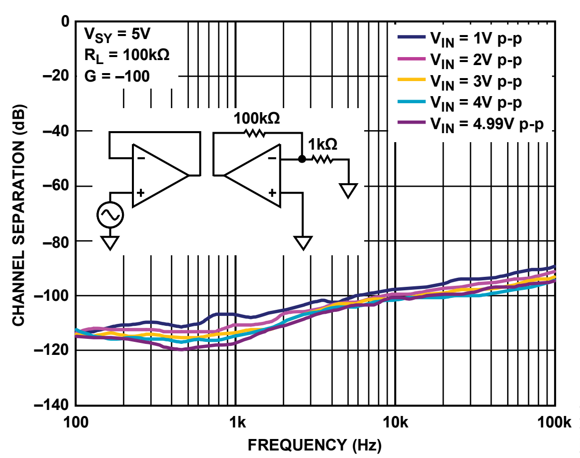



Figure 47. Channel Separation vs. Frequency

$T_A$ = 25°C, unless otherwise noted.

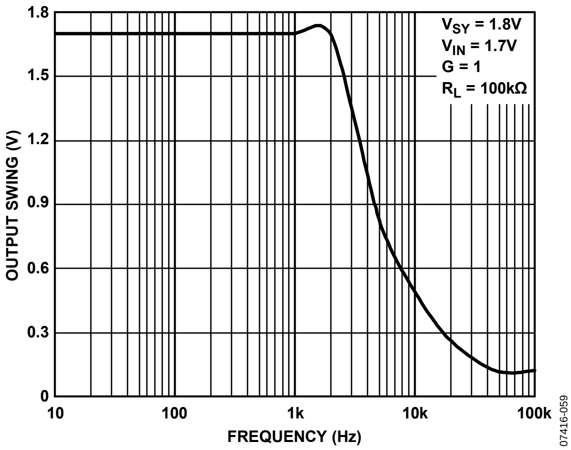



Figure 48. Output Swing vs. Frequency

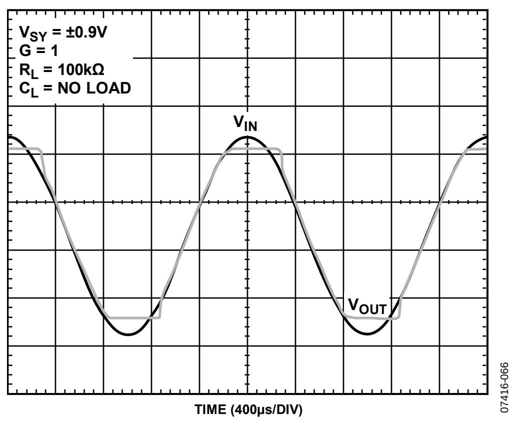



Figure 49. No Phase Reversal

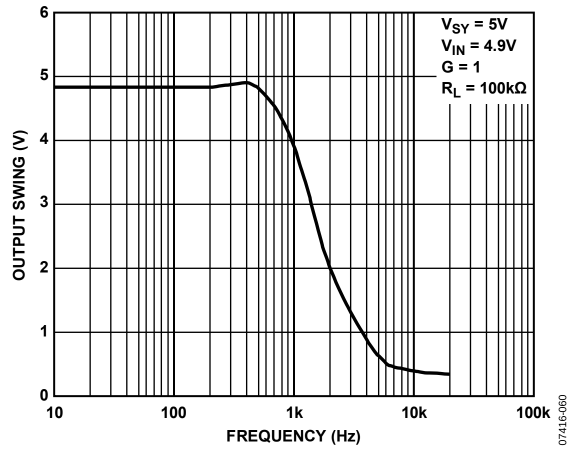



Figure 50. Output Swing vs. Frequency

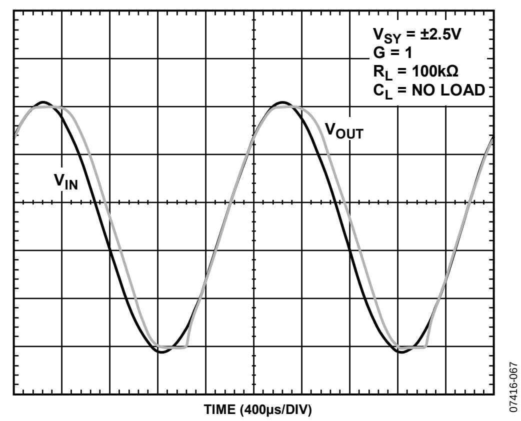



Figure 51. No Phase Reversal

# THEORY OF OPERATION

The ADA4505-1/ADA4505-2/ADA4505-4 are unity-gain stable CMOS rail-to-rail input/output operational amplifiers designed to optimize performance in current consumption, PSRR, CMRR, and zero crossover distortion, all embedded in a small package. The typical offset voltage is 500 μV, with a low peak-to-peak voltage noise of 2.95 μV from 0.1 Hz to 10 Hz and a voltage noise density of 65 nV/√Hz at 1 kHz.

The ADA4505-x amplifiers are designed to solve two key problems in low voltage battery-powered applications: battery voltage decrease over time and rail-to-rail input stage distortion.

In battery-powered applications, the supply voltage available to the IC is the voltage of the battery. Unfortunately, the voltage of a battery decreases as it discharges itself through the load. This voltage drop over the lifetime of the battery causes an error in the output of the op amps. Some applications requiring precision measurements during the entire lifetime of the battery use voltage regulators to power up the op amps as a solution. If a design uses standard battery cells, the op amps experience a supply voltage change from roughly 3.2 V to 1.8 V during the lifetime of the battery. This means that for a PSRR of 70 dB minimum in a typical op amp, the input-referred offset error is approximately 440 μV. If the same application uses the ADA4505-x with a 100 dB minimum PSRR, the error is only 14 μV. It is possible to calibrate this error out or to use an external voltage regulator to power the op amp, but these solutions can increase system cost and complexity. The ADA4505-x amplifiers solve the impasse with no additional cost or error-nullifying circuitry.

The second problem with battery-powered applications is the distortion caused by the standard rail-to-rail input stage. Using a CMOS nonrail-to-rail input stage (that is, a single differential pair) limits the input voltage to approximately one $V_{GS}$ (gate-source voltage) away from one of the supply lines. Because $V_{GS}$ for normal operation is commonly over 1 V, a single differential pair, input stage op amp greatly restricts the allowable input voltage range when using a low supply voltage. This limitation restricts the number of applications where the nonrail-to-rail input op amp was originally intended to be used. To solve this problem, a dual differential pair input stage is usually implemented (see Figure 52); however, this technique has its own drawbacks.

One differential pair amplifies the input signal when the common-mode voltage is on the high end, whereas the other pair amplifies the input signal when the common-mode voltage is on the low end. This method also requires control circuitry to operate the two differential pairs appropriately. Unfortunately, this topology leads to a very noticeable and undesirable problem; if the signal level moves through the range where one input stage turns off and the other one turns on, noticeable distortion occurs (see Figure 53).

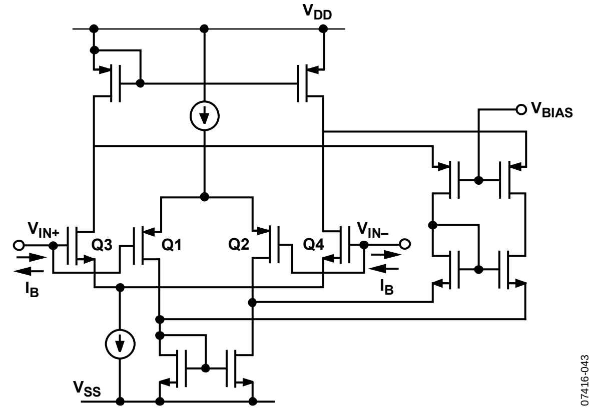



*Figure 52. Typical Dual Differential Pair Input Stage Op Amp (Dual PMOS Q1 and Q2 Transistors Form the Lower End of the Input Voltage Range; Dual NMOS Q3 and Q4 Transistors Form the Upper End)*

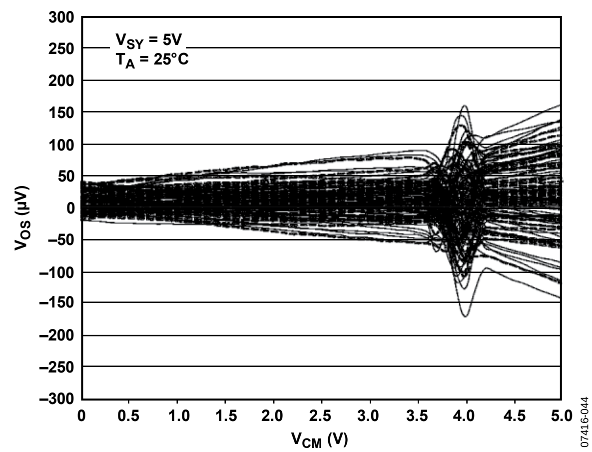



*Figure 53. Typical Input Offset Voltage vs. Common-Mode Voltage Response in a Dual Differential Pair Input Stage Op Amp (Powered by a 5 V Supply; Results of Approximately 100 Units per Graph Are Displayed)*

This distortion forces the designer to devise impractical ways to avoid the crossover distortion areas, thereby narrowing the common-mode dynamic range of the operational amplifier. The ADA4505-x family solves this crossover distortion problem by using an on-chip charge pump to power the input differential pair. The charge pump creates a supply voltage higher than the voltage of the battery, allowing the input stage to handle a wide range of input signal voltages without using a second differential pair. With this solution, the input voltage can vary from one supply extreme to the other with no distortion, thereby restoring the full common-mode dynamic range of the op amp.

The charge pump has been carefully designed so that switching noise components at any frequency, both within and beyond the amplifier bandwidth, are much lower than the thermal noise floor. Therefore, the spurious-free dynamic range (SFDR) is limited only by the input signal and the thermal or flicker noise. There is no intermodulation between input signal and switching noise.

Figure 54 displays a typical front-end section of an operational amplifier with an on-chip charge pump.

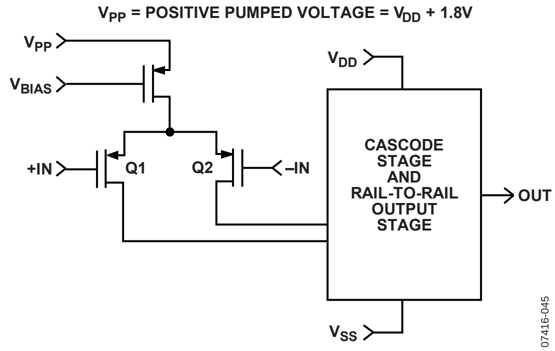



*Figure 54. Typical Front-End Section of an Op Amp with Embedded Charge Pump*

Figure 55 shows the typical response of two devices from Figure 11, which shows the input offset voltage vs. input common-mode voltage for 10 devices. Figure 55 is expanded to make it easier to compare with Figure 53, which shows the typical input offset voltage vs. common-mode voltage response in a dual differential pair input stage op amp.

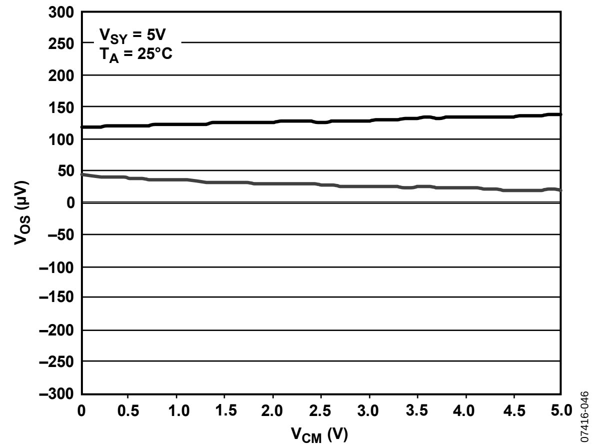



*Figure 55. Input Offset Voltage vs. Input Common-Mode Voltage Response (Powered by a 5 V Supply; Results of Two Units Are Displayed)*

This solution improves the CMRR performance tremendously. For example, if the input varies from rail to rail on a 2.5 V supply rail, using a part with a CMRR of 70 dB minimum, an input-referred error of 790 µV is introduced. Another part with a CMRR of 52 dB minimum generates a 6.3 mV error. The ADA4505-x family CMRR of 90 dB minimum causes only a 79 µV error. As with the PSRR error, there are complex ways to minimize this error, but the ADA4505-x family solves this problem without incurring unnecessary circuitry complexity or increased cost.

# APPLICATIONS INFORMATION

## PULSE OXIMETER CURRENT SOURCE

A pulse oximeter is a noninvasive medical device used for continuously measuring the percentage of hemoglobin (Hb) saturated with oxygen and the pulse rate of a patient. Hemoglobin that is carrying oxygen (oxyhemoglobin) absorbs light in the infrared (IR) region of the spectrum; hemoglobin that is not carrying oxygen (deoxyhemoglobin) absorbs visible red (R) light. In pulse oximetry, a clip containing two LEDs (sometimes more, depending on the complexity of the measurement algorithm) and the light sensor (photodiode) is placed on the finger or earlobe of the patient. One LED emits red light (600 nm to 700 nm), and the other emits light in the near IR (800 nm to 900 nm) region. The clip is connected by a cable to a processor unit. The LEDs are rapidly and sequentially excited by two current sources (one for each LED) whose dc levels depend on the LED being driven, based on manufacturer requirements; the detector is synchronized to capture the light from each LED as it is transmitted through the tissue.

An example design of a dc current source driving the red and infrared LEDs is shown in Figure 56. These dc current sources allow 62.5 mA and 101 mA to flow through the red and infrared LEDs, respectively. First, to prolong battery life, the LEDs are driven only when needed. One third of the ADG733 SPDT analog switch is used to disconnect/connect the 1.25 V voltage reference from/to each current circuit. When driving the LEDs, the ADR1581 1.25 V voltage reference is buffered by one half of the ADA4505-2; the presence of this voltage on the noninverting input forces the output of the op amp (due to the negative feedback) to maintain a level that causes its inverting input to track the noninverting pin. Therefore, the 1.25 V appears in parallel with the 20 Ω R1 or 12.4 Ω R5 current source resistor, creating the flow of the 62.5 mA or 101 mA current through the red or infrared LED as the output of the op amp turns on the Q1 or Q2 N-MOSFET IRLMS2002.

The maximum total quiescent currents for one half of the ADA4505-2, the ADR1581, and the ADG733 are 15 µA, 70 µA, and 1 µA, respectively, for a total of 86 µA current consumption (430 µW power consumption) per circuit, which is good for a system powered by a battery. If the accuracy and temperature drift of the total design need improvement, use a more accurate and low temperature coefficient drift voltage reference and current source resistor. C3 and C4 are used to improve stabilization of U1; R3 and R7 are used to provide some current limit into the U1 inverting pin; and R2 and R6 are used to slow the rise time of the N-MOSFET when it turns on. These elements may not be needed, or some bench adjustments may be required.

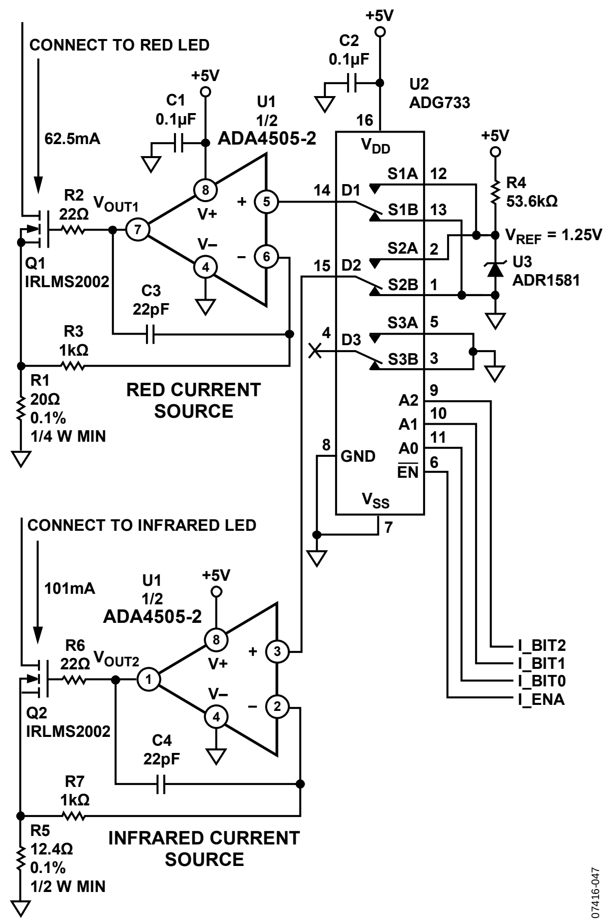



*Figure 56. Pulse Oximeter Red and Infrared Current Sources Using the ADA4505-2 as a Buffer to the Voltage Reference Device*

## FOUR-POLE, LOW-PASS BUTTERWORTH FILTER FOR GLUCOSE MONITOR

There are several methods of glucose monitoring: spectroscopic absorption of infrared light in the 2 μm to 2.5 μm range, reflectance spectrophotometry, and the amperometric type using electrochemical strips with glucose oxidase enzymes. The amperometric type generally uses three electrodes: a reference electrode, a control electrode, and a working electrode. Although this is a very old and widely used technique, signal-to-noise ratio and repeatability can be improved using the ADA4505-x family, with its low peak-to-peak voltage noise of 2.95 μV from 0.1 Hz to 10 Hz and voltage noise density of 65 nV/√Hz at 1 kHz.

Another consideration is operation from a 3.3 V battery. Glucose signal currents are usually less than 3 μA full scale; therefore, the I-to-V converter requires low input bias current. The ADA4505-x family is an excellent choice because it provides 0.5 pA typical and 2 pA maximum input bias current at ambient temperature.

A low-pass filter with a cutoff frequency of 80 Hz to 100 Hz is desirable in a glucose meter device to remove extraneous noise; this can be a simple two-pole or four-pole Butterworth filter. Low power op amps with bandwidths of 50 kHz to 500 kHz should be adequate. The ADA4505-x family, with its 50 kHz GBP and 7 μA typical current consumption, meets these requirements. A circuit design of a four-pole Butterworth filter (preceded by a one-pole low-pass filter) is shown in Figure 57. With a 3.3 V battery, the total power consumption of this design is 198 μW typical at ambient temperature.

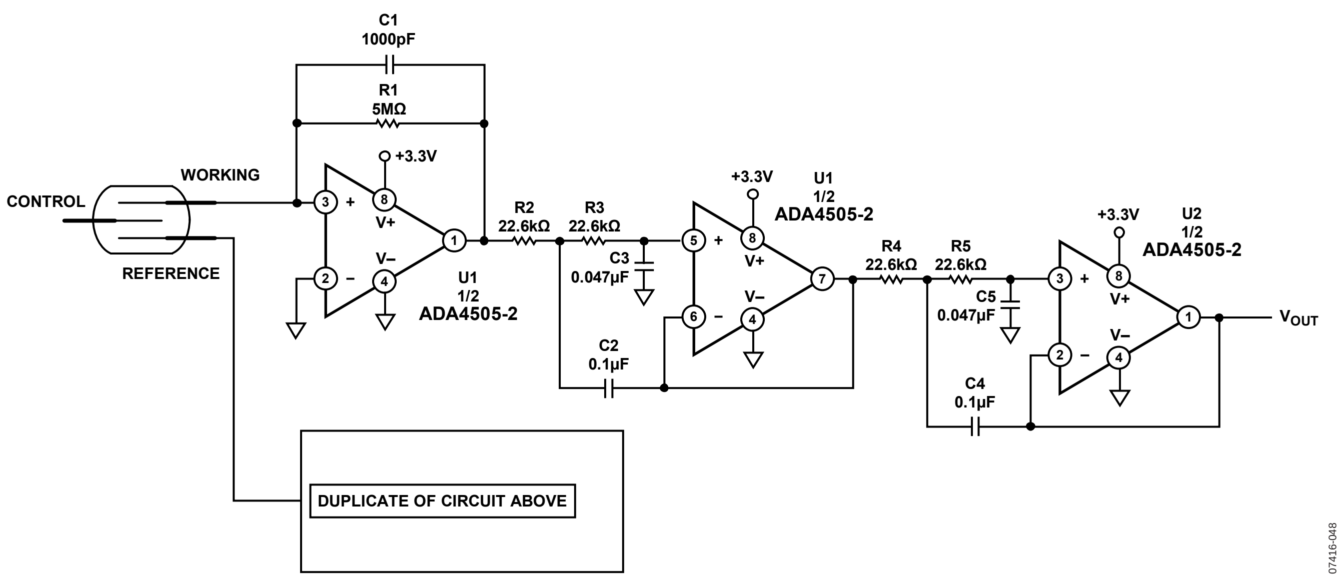



*Figure 57. Four-Pole Butterworth Filter That Can Be Used in a Glucose Meter*

# OUTLINE DIMENSIONS

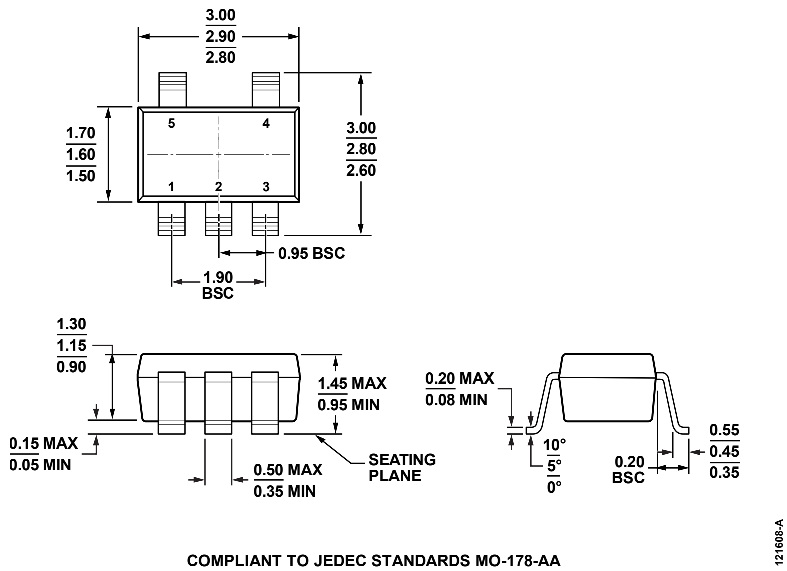



*Figure 58. 5-Lead Small Outline Transistor Package [SOT-23]*
*(RJ-5)*
*Dimensions shown in millimeters*

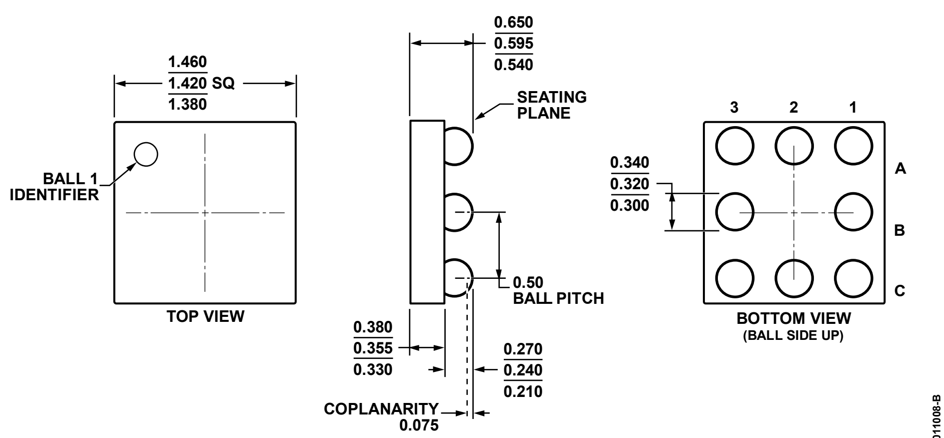
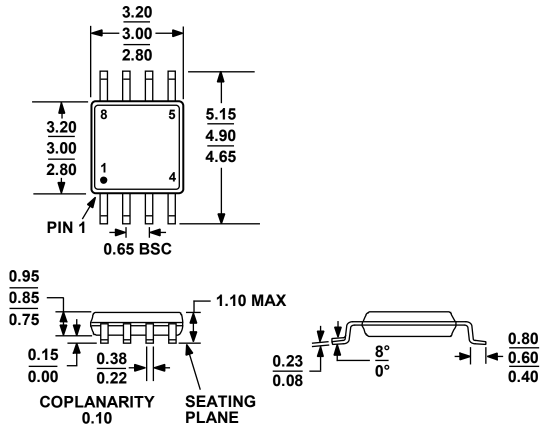
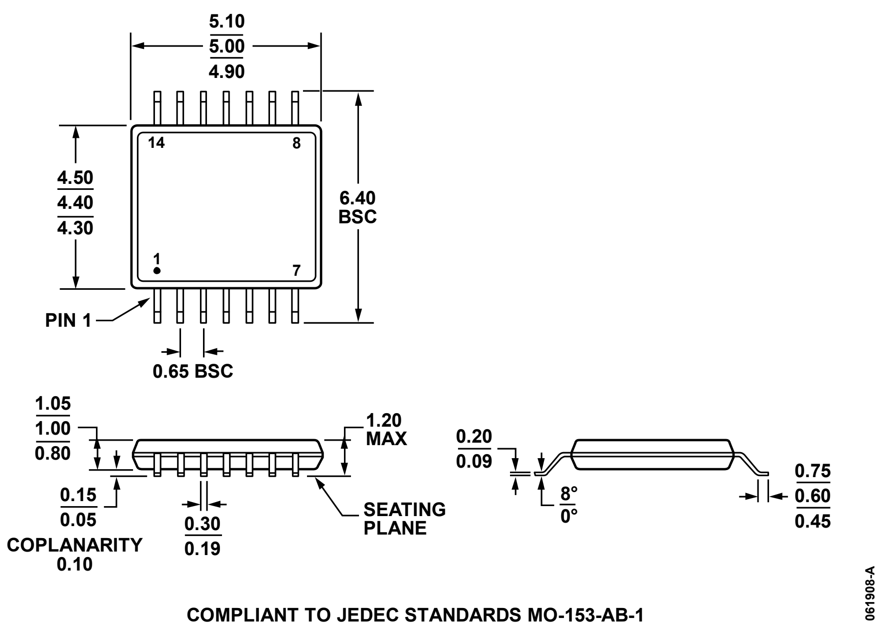



*Figure 59. 8-Ball Wafer Level Chip Scale Package [WLCSP]*
*(CB-8-2)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-187-AA

*Figure 60. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

*Figure 61. 14-Lead Thin Shrink Small Outline Package [TSSOP]*
*(RU-14)*
*Dimensions shown in millimeters*

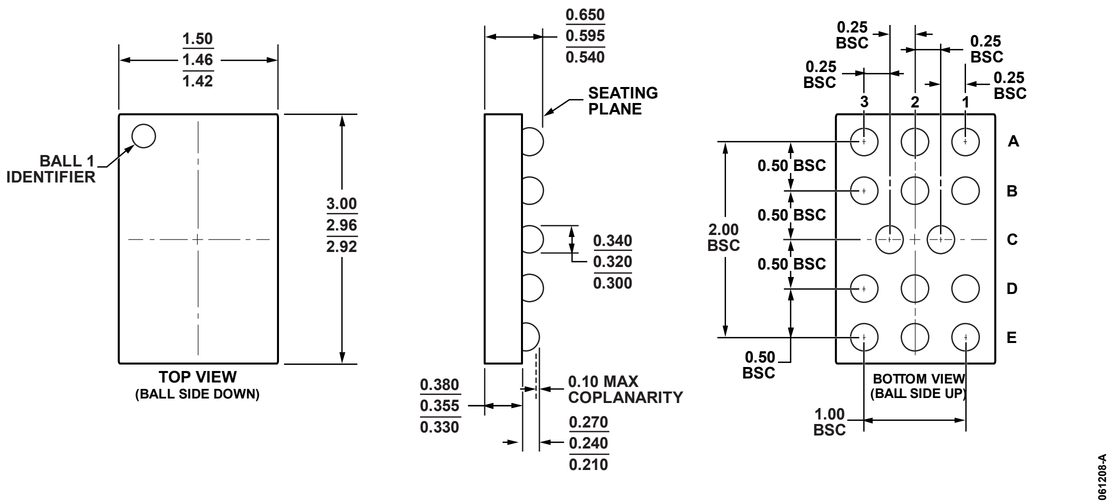



*Figure 62. 14-Ball Wafer Level Chip Scale Package [WLCSP]*
*(CB-14-1)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| ADA4505-1ARJZ-R2[1] | −40°C to +125°C | 5-Lead SOT-23 | RJ-5 | A2D |
| ADA4505-1ARJZ-RL[1] | −40°C to +125°C | 5-Lead SOT-23 | RJ-5 | A2D |
| ADA4505-1ARJZ-R7[1] | −40°C to +125°C | 5-Lead SOT-23 | RJ-5 | A2D |
| ADA4505-2ACBZ-RL[1] | −40°C to +125°C | 8-Ball WLCSP | CB-8-2 | A21 |
| ADA4505-2ACBZ-R7[1] | −40°C to +125°C | 8-Ball WLCSP | CB-8-2 | A21 |
| ADA4505-2ARMZ[1] | −40°C to +125°C | 8-Lead MSOP | RM-8 | A21 |
| ADA4505-2ARMZ-RL[1] | −40°C to +125°C | 8-Lead MSOP | RM-8 | A21 |
| ADA4505-4ARUZ[1] | −40°C to +125°C | 14-Lead TSSOP | RU-14 | |
| ADA4505-4ARUZ-RL[1] | −40°C to +125°C | 14-Lead TSSOP | RU-14 | |
| ADA4505-4ACBZ-RL[1] | −40°C to +125°C | 14-Ball WLCSP | CB-14-1 | A2A |
| ADA4505-4ACBZ-R7[1] | −40°C to +125°C | 14-Ball WLCSP | CB-14-1 | A2A |

[1] Z = RoHS Compliant Part.


D07416-0-7/09(C)